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Amendments to the Specification

Please replace Paragraphs [0032], [0035], and [0037] with the following amended paragraphs. All amendments are shown with deleted text strikethrough or double bracketed and new text underlined.

[0032] The filtered versions of the real and imaginary data are then rotated by complex rotator 602 by a phase angle factor. Rotator 604 [[603]] is preferably a complex multiplier which allows the noise shaping function of the D/A conversion to track the center frequency of the clock being generated. Rotator 602 could be, for example, based on a look-up table in ROM storing real and imaginary rotated parts. For example, the 3 MSBs of each of the real and imaginary parts could be concatenated with a 6-bit phase angle to produce addresses to the ROM. Rotator 602, as well as rotator 604 [[603]], can also be constructed from a combination of ROM, adders and multiplexers.

[0035] Backend BFPs 403 reduce noise from the synthesized analog sine and cosine signals to control jitter in the final output clock. In the preferred embodiment, at least the final stages of these filters are continuous time filters. Using continuous time filters constructed from tunable transconductances and capacitors is one approach. These filters can be based on one or more cascaded resonators such as resonator 700 shown in FIGURE 7A. Resonator 700 includes cross-coupled real and imaginary paths based on tunable transconductances 701-703, capacitors 704 [[804]] and amplifiers 705 [[804]]. In this example, if the center frequency being generated is f, then:

(1) $2\pi f = g_{m3} / C$ then

(2) $g_{m1} = g_{m2} = g_{m3} / Q$,

where a resonator Q of 5 – 20 will be sufficient for filters using 1 – 3 resonator stages 700 [[800]].

[0037] FIGURE 8 shows one possible embodiment of a back-end phase-locked loop 800 suitable for generating the final digital clock in block 206 from the filtered analog signal. Here, the output from voltage controlled oscillator (VCO) 801 is divided in block 802 by a divisor n (e.g. 4, 8, 10, and so on) to generate a "gray code" of two out 90-degree out of phase digital clocks forming a complex clock signal. The complex clock signal is optionally filtered by bandpass filter (BPF) 803 and then convolved by a complex reference signal by multiplier 805 and filtered by low pass filter 806. The result is a low frequency that is feedback to front-end phase (frequency) detector 807 [[805]] at the voltage control input to VCO 801, where it is compared against the real and imaginary parts of the synthesized analog clock waveform. The final output digital clock has only a small amount of additional noise from the convolution. More importantly, there is little, if any, reference feed-through.